PPA Evaluation of BS-PDN Compared to FS-PDN in the Early Stage

Dean Huang, Andy Wei, Chee How Lim, Yi Wei Chen
Intel

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Agenda

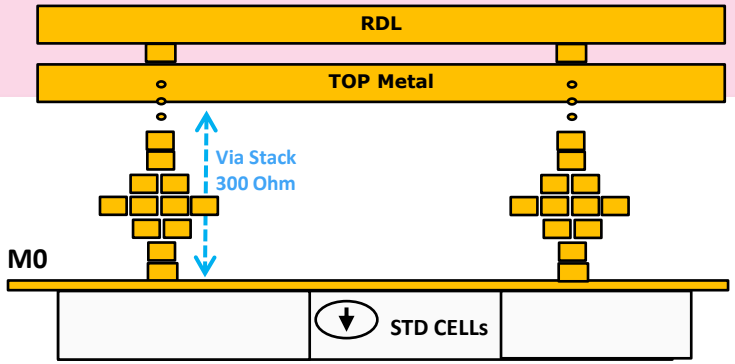
- Background
- Motivation
- Main Idea
- Case Study
- Summary

Background: BSPDN Enhance PPA

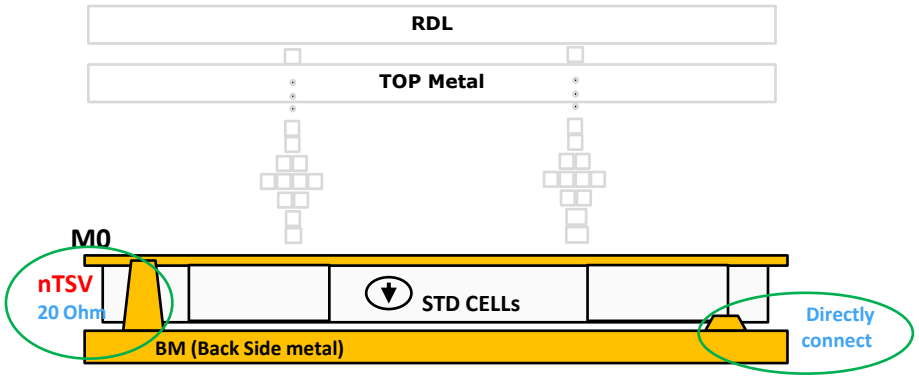
- **F**ront **S**ide **P**ower **D**eliver **N**etwork: (FS-PDN)
  - Traditional Power Deliver Network formed by Vias and metals
  - Occupied 30% metal routing resource that shared with signal route
  - Higher IR drop: The increase in the number of metal layers and the reduction in via diameter result in higher resistance

- **B**ack **S**ide **P**ower **D**eliver **N**etwork: (BS-PDN)
  - Advanced PDN
  - By relocating the PDN to the backside of the substrate, free up routing resources for signal routing to achieve better performance
  - One of the BSPDN process is adopting nTSV inside the power tap cell to connect M0 from BM (Backside Metal)
  - The other BSPDN without nTSV, BM directly connected to device
  - Lower IR drop: Due to Via Stack is replaced by nTSV and decrease in vertical resistance from 300 Ohms to 20 Ohms **

FSPDN



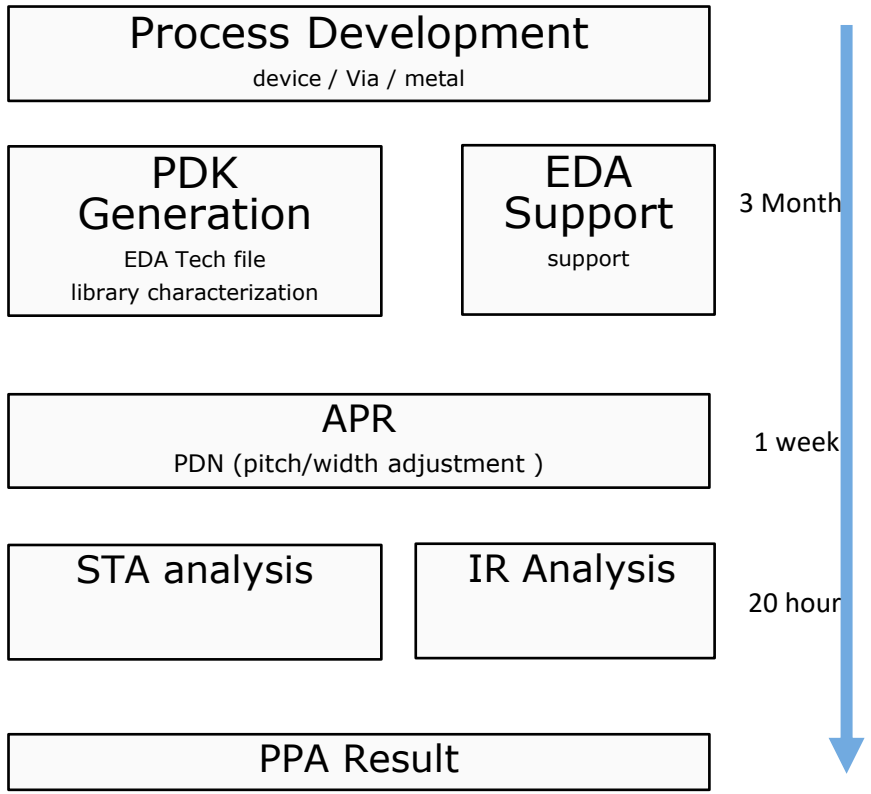
BSPDN



** To prevent the disclosure of sensitive process parameters, all process parameters and resistances are substituted with non-sensitive values.

Motivation: How to Evaluate PPA of BSPDN at Early Stage

- Problem: PPA evaluation need PDK/EDA flow, and it takes long time



- If PDK and EDA can be ready, we can evaluate PPA at early stage
- The PPA result can help the selection of process and feedback to process R&D team for further DTCO

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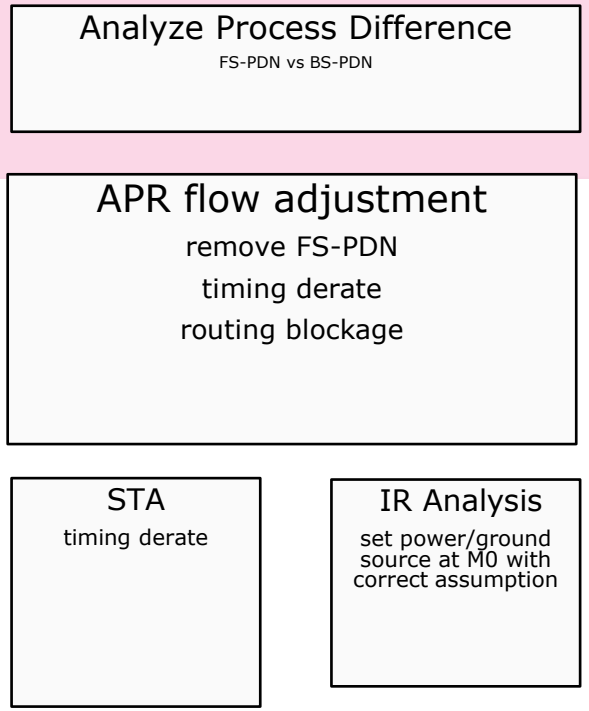
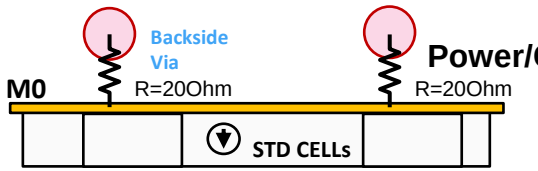
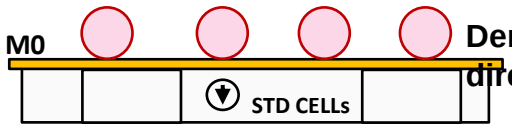
Main Idea: Hack exist PDK and EDA flow to evaluate BSPDN

- According to exist FS-PDN PDK and EDA flow
- Analyze the difference of process between FS-PDN and BS-PDN
  - library cell area (width/height)
  - library cells performance
  - Routing track difference
- APR Flow Adjustment by the analysis results
  - Remove PDN to simulate BS-PDN
  - set timing derate on library cells (if device performance changed)
  - Create routing blockage according to routing track differences if necessary
- STA
  - set timing derate on cells (if device performance changed)
- IR analysis
  - BM is thick metal with low resistance, hence can be assume as ideal voltage source
  - BSPDN with nTSV
    - create power/ground source at M0 according to the nTSV pitch, each bump with nTSV resistance
  - BSPDN without nTSV (BM direct connect to device)
    - create power/ground source at M0 with dense pitch





Power/Ground Bump attached to M0



Dense Power/Ground Bump at M0 directly

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Case Study: Flow Adjustment Example

Design	Arm A55 Dpu module
Speed	4.0 Ghz
Process	< 10 nm **
Power	27 mW
Metal #	18M
Size	120 x 120 (um)
Instance Count	130K

- BS-PDN analysis results :
  - Same cell library with FS-PDN
  - No timing change in standard cell
  - No size change in standard cell
  - M1 Routing track reduced due to nTSV every 6 tracks

APR (Auto Place&Route) adjustment

- BS-PDN implementation
  - Remove FS-PDN mesh in original flow
  - place/cts/route engine will take advantage of those routing tracks released
- Routing Track adjustment
  - Create M1 routing track blockage every 6 tracks
- Place/CTS/Route flow adjustment
  - in general case, no flow need to be adjusted

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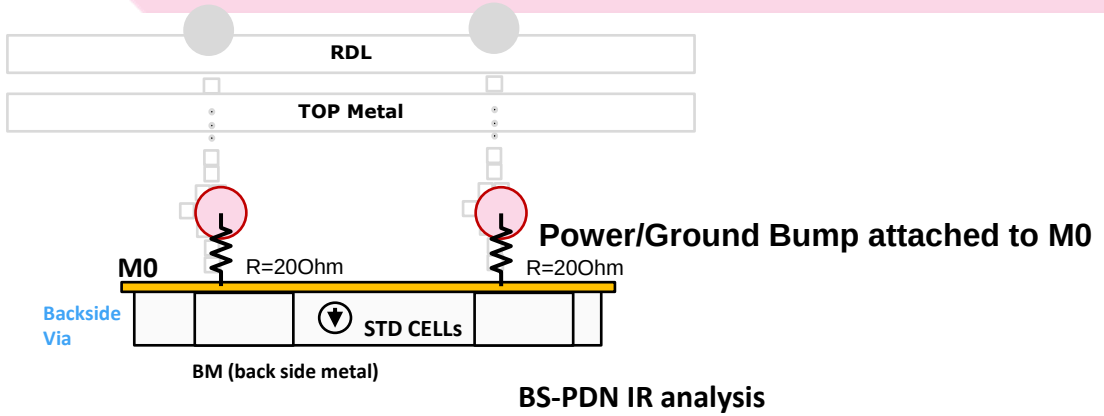
Case Study: Flow Adjustment Example

Timing/IR Analysis

- STA (Static Timing Analysis)
  - if timing of standard cells changed, adjust margin/derate setting in EDA tools. Ex. all cells scale up 1.05x (at both APR/STA tools)
  - in this case, keep the same
- IR Analysis
  - FS-PDN is removed, and the power supply is from back-side
  - In EDA IR analysis, BS-PDN can be formed use bump resistance to attach bump to M0 as below
  - Use bump/power source description file in IR tools to add power source directly attached to M0 along with a reasonable resistance
  - ** The IR drop on BM can be ignored. Backside metal is a thick metal with low resistance



BS-PDN IR analysis

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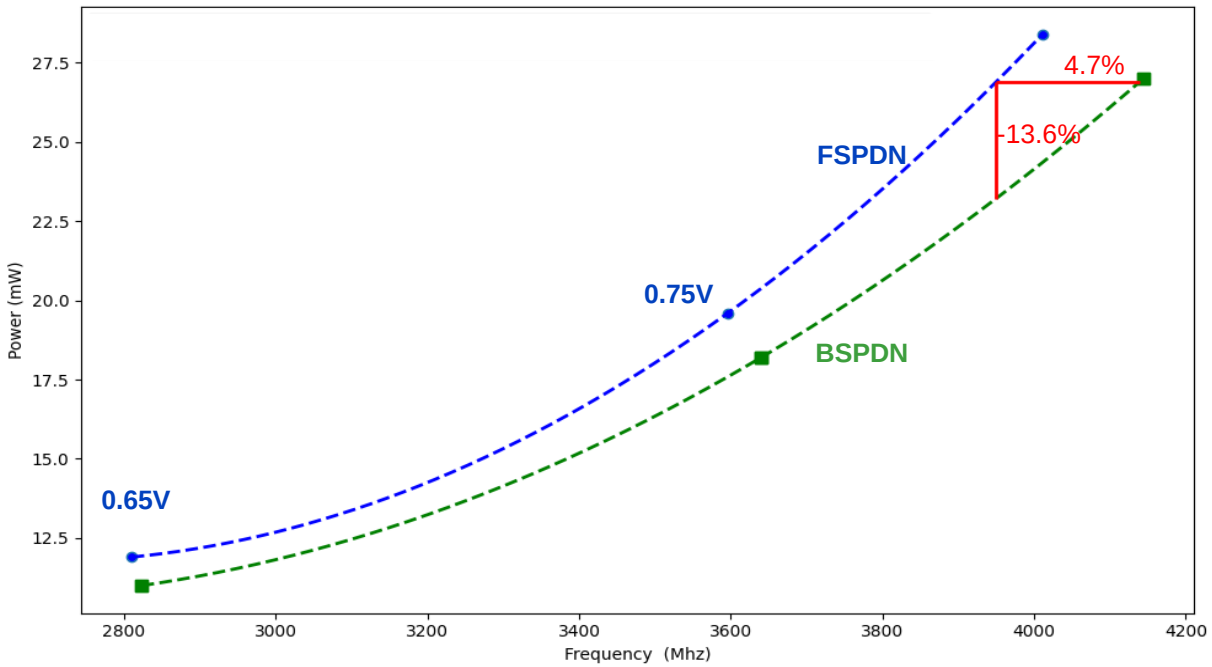
Case Study: PPA / IR evaluation result of FSPDN vs BSPDN

Design	Arm A55 Dpu module
Speed	4.0 Ghz
Process	< 10 nm **
Power	27 mW
Metal #	18M
Size	120 x 120 (um)
Instance Count	130K

	Frequency @ same power	Power @ same-frequency
BSPDN Enhancement	4.70%	-13.60%

Result:

- 4.7% frequency gain at same power and -13.6% power reduction at same frequency
- Area can be reduced 4% if keep same design performance spec



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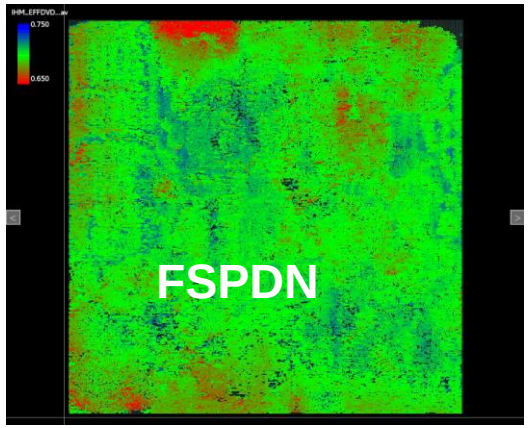
Case Study: PPA / IR evaluation result of FSPDN vs BSPDN

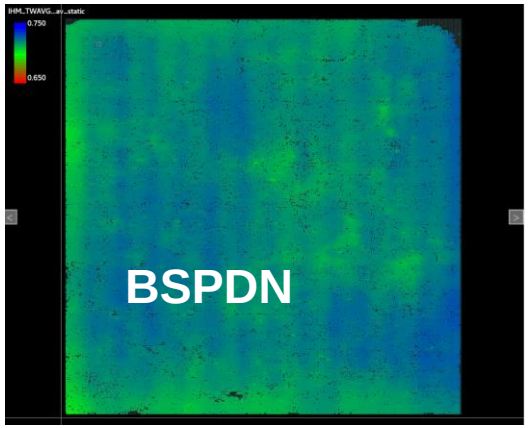
	Static IR drop (%)	Dynamic IR drop (%)
FSPDN	4.10%	15.70%
BSPDN	1.30%	5.30%

Result:

- Static IR drop from 4.1% to 1.3%. Dynamic IR 15.7% to 5.3%

IR heat map





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Summary and Future Work

- This work present a methodology to evaluate PPA of BSPDN before PDK/EDA flow is ready
  - Benefit process selection
  - Feedback to BS-PDN to do more DTCO
- PPA gain of replacing FS-PDN to BS-PDN in this simple case is 4.7% in frequency and -13.6% in power
- IR drop enhance 4.1% to be 1.3% in static IR, 15.7% to be 5.3% in dynamic IR. Those improvement can be benefit to PPA further
  - Ex. release more timing guard band due to IR drop reduced and higher performance can be achieved
  - or lower supply voltage guard band to save more power
- Design with power switch is not considered but can estimated by adding more IR drop margin
- In general case, we can find same cell height FSPDN library, but if we can't find one. It's more complicated for EDA tools to hack library cell height. The better way is to estimate PPA gain in 3 part
  - 1, Estimate PPA gain of cell height change in FS-PDN
  - 2, Estimate PPA gain of FS-PDN to BS-PDN
  - 3, accumulate Part1 + Part2
- Future work, will compare the PPA result when final PDK/EDA tools is ready.

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